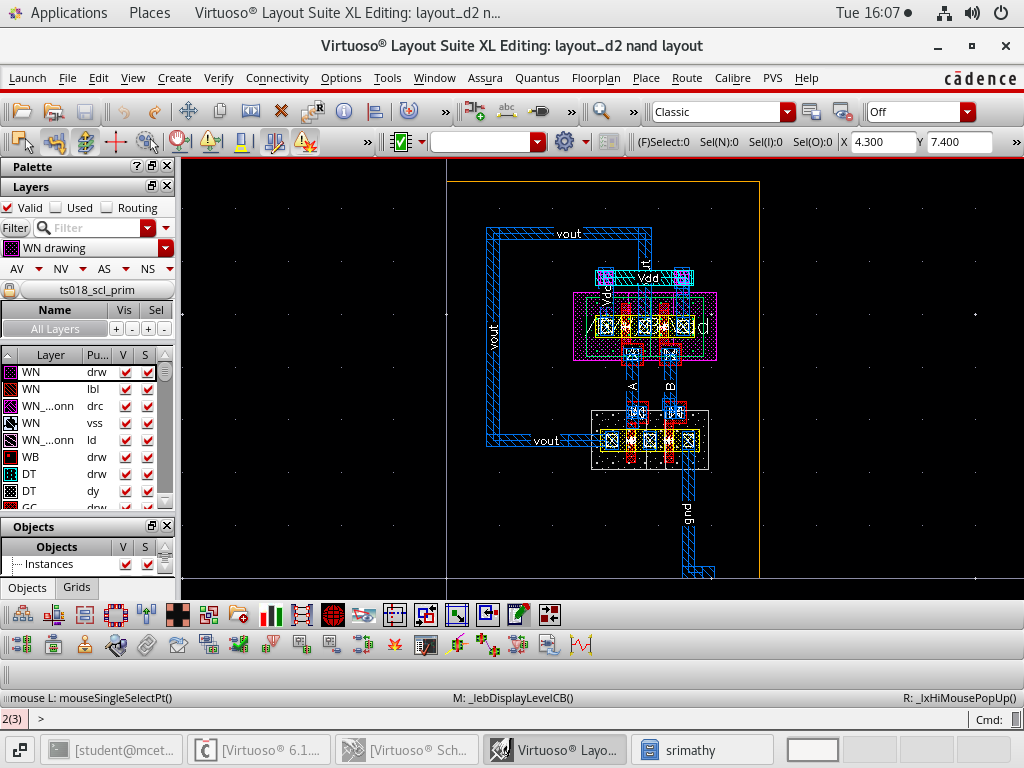
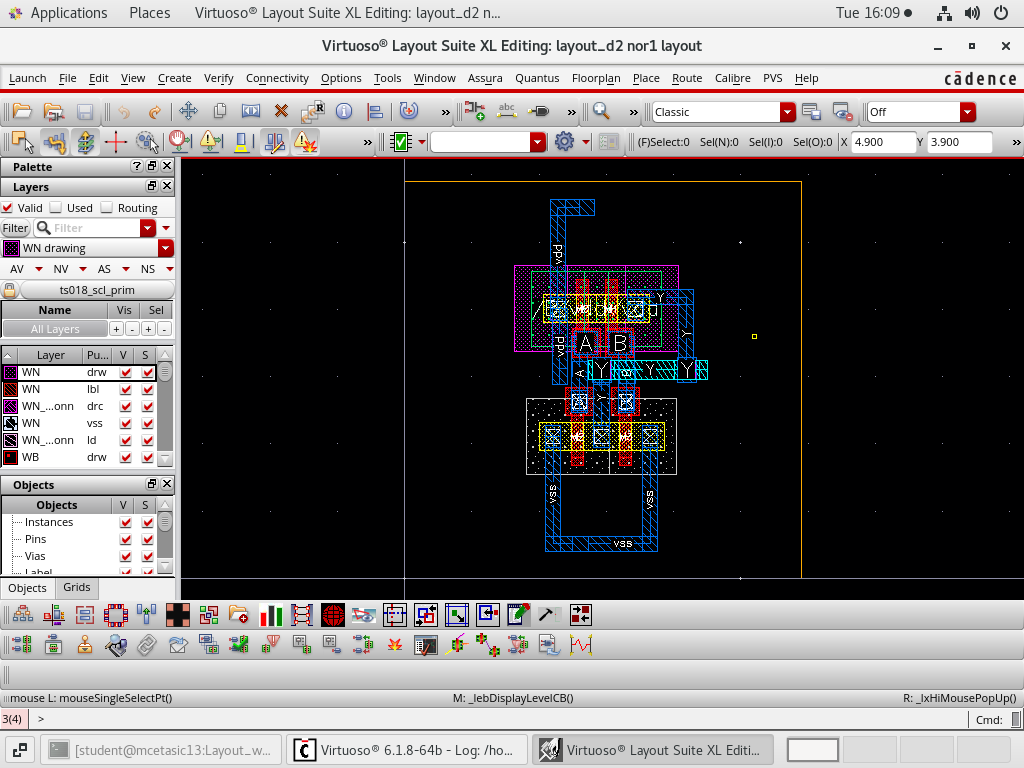
**EXP.NO:9**

**CMOS NAND LAYOUT:**



**CMOS NOR LAYOUT:**



**EXP.NO:10**

**4 BIT RIPPLE CARRY ADDER:**

**RIPPLE CARRY ADDER:**

module rca(

input [3:0] a,

input [3:0] b,

input cin,

wire[2:0] w,

output [3:0] s,

output cout

);

FA fa01(a[0],b[0],cin,s[0],w[0]);

FA fa02(a[1],b[1],w[0],s[1],w[1]);

FA fa03(a[2],b[2],w[1],s[2],w[2]);

FA fa04(a[3],b[3],w[2],s[3],cout);

endmodule

module FA(

input a,b,c,

output sum,

output carry

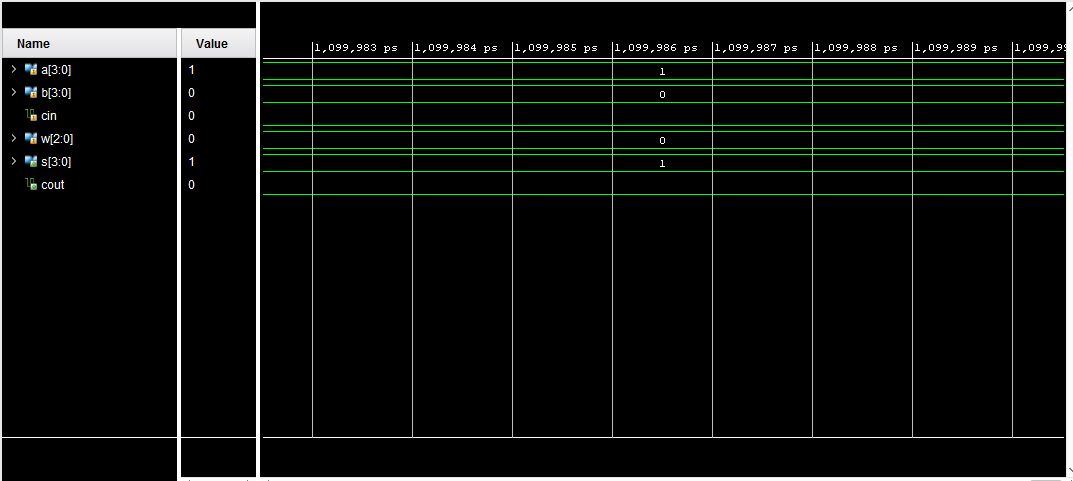
);

assign sum = a^b^c;

assign carry = (a&b)|(b&c)|(a&c);

endmodule

**OUTPUT:**



**D FLIPFLOP:**

module d\_flipflop(

input d,

input clk,

input rest,

output reg q

);

always@(posedge clk)

begin

if(rest==1'b1)

q<=1'b0;

else

q<=d;

end

endmodule

**OUTPUT:**

